WHAT IS CLAIMED IS:

1. A semiconductor device comprising a DRAM region and a high-speed CMOS logic region that are co-resident with each other,

wherein a pair of gate electrodes of a N-type sense amplifier transistor and a pair of gate electrodes of a P-type sense amplifier transistor constituting a CMOS sense amplifier of the DRAM are disposed respectively in one active region in parallel to each other in the same direction as that of bit lines, and a pair of adjacent N-type sense amplifier transistors and a pair of adjacent P-type sense amplifier transistors are isolated by shallow trench isolation (STI) regions.

2. The semiconductor device according to claim 1, wherein floating electrodes are disposed on the shallow trench isolation regions between the pair of adjacent N-type sense amplifier transistors and between the pair of adjacent P-type sense amplifier transistors so as to be parallel to the pair of gate electrodes of each of the sense amplifier transistors.

3. The semiconductor device according to claim 2, wherein the pair of gate electrodes and the floating electrodes are disposed at a substantially equal interval.

4. A semiconductor device comprising a DRAM region and a high-speed CMOS logic region that are co-resident with each other,

wherein a pair of gate electrodes of a N-type sense amplifier transistor and a pair of gate electrodes of a P-type sense amplifier transistor constituting a CMOS sense amplifier of the DRAM are disposed respectively in one active region in parallel to each other in the same direction as that of bit lines, active regions are connected to each other in a pair of adjacent N-type sense amplifier transistors and a pair of adjacent P-type sense amplifier transistors, and on the active regions, field shield electrodes are disposed between the pair of adjacent N-type sense amplifier transistors and between the pair of adjacent P-type sense amplifier transistors so as to be parallel to the pair of gate electrodes of each of the sense amplifier transistors.

5. The semiconductor device according to claim 4, wherein the pair of gate

electrodes and the field shield electrodes are disposed at a substantially equal interval.

6. The semiconductor device according to claim 4, wherein a negative voltage used for a ground potential or a substrate potential of a DRAM cell is applied to the field shield electrodes on the N-type active regions.

7. A semiconductor device comprising a DRAM region and a high-speed CMOS logic region that are co-resident with each other,

wherein a pair of gate electrodes of a N-type sense amplifier transistor and a pair of gate electrodes of a P-type sense amplifier transistor constituting a CMOS sense amplifier of the DRAM are disposed respectively in one active region in parallel to each other in the same direction as that of bit lines, active regions are connected to each other in a pair of adjacent N-type sense amplifier transistors, on the active regions, a field shield electrode is disposed between the pair of adjacent N-type sense amplifier transistors so as to be parallel to the pair of gate electrodes of the N-type sense amplifier transistor, a pair of adjacent P-type sense amplifier transistors are isolated by shallow trench isolation (STI) regions, and a floating electrode is disposed on the shallow trench isolation region between the pair of P-type sense amplifier transistors so as to be parallel to the pair of gate electrodes of the P-type sense amplifier transistor.

8. The semiconductor device according to claim 7, wherein the pair of gate electrodes of the N-type sense amplifier transistor and the field shield electrodes, and the pair of gate electrodes of the P-type sense amplifier transistor and the floating electrodes are disposed at a substantially equal interval.

9. The semiconductor device according to claim 7, wherein a negative voltage used for a ground potential or a substrate potential of a DRAM cell is applied to the field shield electrodes on the N-type active regions.